CLAIMS

1. An electroplating process comprising electroplating an electrically conductive substrate wherein the electroplating is performed intermittently using said substrate surface as cathode and a plating metal as anode at a constant voltage between said anode and said cathode.

2. The electroplating process according to Claim 1 wherein said intermittent electroplating is performed by repeating application of a voltage between a cathode and an anode and interruption of said application alternately with a voltage time/interruption time ratio of 0.01 to 100, a voltage time of not longer than 10 seconds and an interruption time of not less than $1x10^{-12}$ seconds.

3. A process for producing a circuit board comprising a substrate and, as formed thereon, a conductor circuit by electroplating which is performed intermittently using the electrically conductive conductor circuit-forming surface as cathode and a plating metal as anode at a constant voltage between said anode and said cathode.

4. The process for producing a circuit board according to Claim 3 wherein said intermittent electroplating is performed by repeating application of a voltage between a cathode and an anode and interruption of said application alternately with a voltage time/interruption time ratio of 0.01 to 100, a voltage time of not longer than 10 seconds and an interruption time of not less than $1x10^{-12}$ seconds.

5. A process for manufacturing a printed circuit board which comprises disposing a resist on an electrically conductive layer formed on a substrate, performing electroplating, stripping the resist off and etching said

electrically conductive layer to provide a conductor circuit, wherein the electroplating is performed intermittently using said electrically conductive layer as cathode and a plating metal as cathode at a constant voltage between said anode and said cathode.

6. A process for manufacturing a printed circuit board which comprises disposing an interlayer resin insulating layer on a substrate formed with a conductor circuit, creating openings for formation of via holes in said interlayer resin insulating layer, forming an electroless plated metal layer on said interlayer resin insulating layer, disposing a resist thereon, performing electroplating, stripping the resist off and etching the electroless plated metal layer to provide a conductor circuit and via holes, wherein the electroplating is performed intermittently using said electroless plated metal layer as cathode and a plating metal as anode at a constant voltage between said anode and said cathode.

7. The process for manufacturing a printed circuit board according to Claim 6 wherein said interlayer resin insulation layer has a metal layer on its surface.

8. The process for manufacturing a printed circuit board according to Claim 5, 6 or 7 wherein said intermittent electroplating is performed by repeating application of a voltage and interruption of application alternately with a voltage time/interruption time ratio of 0.01 to 100, a voltage time of not longer than 10 seconds and an interruption time of not less than $1x10^{-12}$ seconds.

9. A circuit board comprising a substrate and, as built thereon, a circuit comprised of a copper film, wherein said copper film has properties that (a) its crystallinity is such that the X-ray diffractiion half-width of the (331) plane of

copper is less than 0.3 deg and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

10. The circuit board according to Claim 9 wherein said copper film has an elongation of not less than 7%.

11. A printed circuit board comprising a substrate and, as built thereon, a circuit comprised of a plated copper film, wherein said plated copper film has properties that (a) its crystallinity is such that the X-ray diffraction half-width of (331) plane of copper is less than 0.3 deg and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said plated copper layer as measured over the whole surface of said substrate is not greater than 0.4.

12. A printed circuit board comprising a substrate formed with a conductor circuit, an interlayer resin insulating layer built thereon and a conductor circuit comprised of a copper film as built on said interlayer resin insulating layer, said interlayer resin insulating layer having vial holes by which said conductor circuits are interconnected, wherein said copper film has properties that (a) its crystallinity is such that the X-ray diffraction half-width of (331) plane of copper is less than 0.3 deg and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

13. The printed circuit board according to Claim 11 or 12 wherein said copper film has an elongation of not less than 7%.

14. An electroless plating solution which comprises an

aqueous solution containing 0.025 to 0.25 mol/L of a basic compound, 0.03 to 0.15 mol/L of a reducing agent, 0.02 to 0.06 mol/L of copper ion and 0.05 to 0.3 mol/L of tartaric acid or a salt thereof.

15. An electroless plating solution which comprises an aqueous solution containing a basic compound, a reducing agent, copper ion, tartaric acid or a salt thereof and at least one metal ion species selected from the group consisting of nickel ion, cobalt ion and iron ion.

16. The electroless plating solution according to Claim 14 or 15 wherein said electroless plating solution has a specific gravity of 1.02 to 1.10.

17. The electroless plating solution according to any of Claims 14 to 16, the temperature of which is 25 to 40℃.

18. The electroless plating solution according to any of Claims 14 to 17 wherein the copper deposition rate of said electroless plating solution is 1 to 2 μm/hour.

19. An electroless plating process which comprises immersing a substrate in the electroless plating solution according to any of Claims 14 to 17 and performing electroless copper plating at a deposition rate set to 1 to 2 μm/hour.

20. The electroless plating process according to Claim 19 wherein said substrate has a roughened surface.

21. A process for manufacturing a printed circuit board which comprises immersing a resin insulating substrate board in the electroless plating solution according to any of Claims 14 to 17 and performing electroless copper plating at a deposition rate set to 1 to 2 μm/hour to provide a conductor

circuit.

22. A printed circuit board comprising a resin insulating substrate board formed with a roughened surface and, as built thereon, a conductor circuit comprising at least an electroless plated film, wherein said electroless plated film has a stress of 0 to +10 kg/mm^2.

23. A printed circuit board comprising a resin insulating substrate board formed with a roughened surface and, as built thereon, a conductor circuit comprising at least an electroless plated film, wherein said electroless plated film is complementary to said roughened surface with the electroless plated film in convex areas of the roughened surface being relatively greater in thickness than said film in concave areas of said roughened surface.

24. A printed circuit board comprising a substrate board formed with a lower-layer conductor circuit and, as built thereon, an upper-layer conductor circuit through the intermediary of an interlayer resin insulating layer, with said upper-layer conductor circuit and said lower-layer conductor circuit being interconnected by via holes,
wherein said upper-layer conductor circuit comprises at least an electroless plated film, said interlayer resin insulating layer is provided with a roughened surface, said electroless plated film is complementary to said roughened surface, and bottoms of said via holes are also provided with an electroless plated film having a thickness equal to 50 to 100% of the thickness of the electroless plated film on said interlayer resin insulating layer.

25. A printed circuit board comprising a resin insulating substrate board and, as built thereon, a conductor circuit comprising at least an electroless plated film,

wherein said electroless plated film comprises copper and at least one metal species selected from the group consisting of nickel, iron and cobalt.

26. The printed circuit board according to Claim 25 wherein the proportion of said at least one metal species selected from the group consisting of nickel, iron and cobalt is 0.1 to 0.5 weight %.

27. A process for manufacturing a multilayer printed circuit board which comprises at least the following steps (1) to (5).

(1) a step for thinning the copper foil of a copper-clad laminate by etching

(2) a step for piercing through holes in said copper-clad laminate

(3) a step for depositing a plated metal film on said copper-clad laminate to construct plated-through holes within said through holes

(4) a step for pattern-etching the copper foil and plated metal film on said copper-clad laminate to construct a conductor circuit

(5) a step for serially building up an interlayer resin insulating layer and a conductor layer alternately over said conductor circuit.

28. A process for manufacturing a multilayer printed circuit board which comprises at least the following steps (1) to (7):

(1) a step for thinning the copper foil of a copper-clad laminate by etching

(2) a step for piercing through holes in said copper-clad laminate

(3) a step for forming a conductor film on said copper-clad laminate

Amendment filed under PCT Article 34.

(4) a step of disposing a resist on the area free from conductor circuits and plated-through holes

(5) a step for providing a plated metal film in the resist-free area to construct a conductor circuit and plated-through holes

(6) a step for stripping off said resist and etching the conductor film and copper foil underneath the resist

(7) a step for serially building up an interlayer resin insulating layer and a conductor layer alternately over said conductor circuit.

29. The process for manufacturing a multilayer printed circuit board according to Claim 27 or 28 wherein a laser is used for piercing the through holes in said copper-clad laminate.

30. The process for manufacturing a multilayer printed circuit board according to Claim 27 or 28 wherein a drill is used for piercing the through holes in said copper-clad laminate.

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31. The process for manufacturing a multilayer printed circuit board according to any of Claims 27 to 30, wherein, in the step for thinning the copper foil of said copper-clad laminate by etching, the thickness of the copper foil is reduced to 1 to 10 μm.

32. (Amended) A multilayer printed circuit board comprising a core board having a conductor circuit and, as built over said conductor circuit, a buildup wiring layers obtainable by building up an interlayer resin insulating layer and a conductor layer alternately with the conductor layers being interconnected by via holes,

wherein said core board comprises a copper-clad laminate , the conductor circuit on said core board comprises the copper

foil of said copper-clad laminate and a plated metal layer, and the thickness of the conductor circuit on said core board is not greater by more than 10 μm than the thickness of the conductor layer on said interlayer resin insulating layer.

33. (Cancelled)

34. A process for manufacturing a multilayer printed circuit board which comprises thinning the copper foil of a copper-clad laminate by etching, pattern-etching the copper foil of said copper-clad laminate to construct a conductor circuit and building up serially an interlayer resin insulating layer and a conductor layer alternately over said conductor circuit wherein the thickness of the conductor circuit on said core board is controlled so as to be not greater by more than 10 μm than the thickness of the conductor layer on said interlayer resin insulating layer.

35. A process for manufacturing a multilayer printed circuit board which comprises constructing an interlayer insulating layer on a substrate formed with a lower-layer conductor circuit, piercing openings in said interlayer insulating layer, imparting electrical conductivity to the surface of said interlayer insulating layer and the inner walls of said openings, performing electroplating to fill up said openings and thereby provide via holes and, at the same time, construct an upper-layer conductor circuit, wherein said electroplating is performed using an aqueous solution containing a metal ion and 0.1 to 1.5 mmol/L of at least one additive selected from the group consisting of a thiourea, a cyanide and a polyalkylene oxide as a plating solution.

36. The process for manufacturing a multilayer printed circuit board according to Claim 35 wherein the aspect ratio

of said openings for via holes, i.e. depth of opening/diameter of opening, is 1/3 to 1/1.

37. A multilayer printed circuit board comprising a core board and, as constructed on both sides thereof, a buildup wiring layers obtainable by building up an interlayer resin insulating layer and a conductor layer alternately with said conductor layers being interconnected by via holes,
wherein said via holes are formed in the manner of plugging the through holes in plated-through holes in said core board.

38. The multilayer printed circuit board according to Claim 37 wherein the through holes in said plated-through holes have a diameter of not more than 200 μm.

39. A process for manufacturing a multilayer printed circuit board which comprises at least the following steps (1) to (4):
(1) a step for piercing through holes not larger than 200 μm in diameter in a core board by laser
(2) a step for plating said through holes therein to construct plated-through holes
(3) a step for constructing an interlayer resin insulating layer provided with openings communicating with said plated-through holes on the core board
(4) a step for plating the openings in said interlayer resin insulating layer to construct via holes in the manner of plugging the through holes in said plated-through holes.

40. A multilayer printed circuit board comprising a core board and, as constructed on both sides thereof, a buildup wiring layers obtainable by building up an interlayer resin insulating layer and a conductor layer alternately with via holes interconnecting conductor layers,
wherein the via holes in a lower layer are disposed immediately

over the plated-through holes in said core board and via holes in an upper layer are disposed immediately over said via holes in the lower layer.

41. A multilayer printed circuit board comprising a core board and, as constructed on both sides thereof, a buildup wiring layers obtainable by building up an interlayer resin insulating layer and a conductor layer alternately with via holes interconnecting conductor layers,
wherein said plated-through holes of core board are filled with a filler, with the surfaces of said filler which are exposed from said plated-through holes being covered with a conductor layer provided with lower-layer via holes and upper-layer via holes being disposed immediately over said lower-layer via holes.

42. A multilayer printed circuit board comprising a core board and, as constructed on both sides thereof, a buildup wiring layers obtainable by building up an interlayer resin insulating layer and a conductor layer alternately with via holes interconnecting conductor layers,
wherein via holes in a lower layer are disposed to plug the through holes of plated-through holes in said core board, with via holes in an upper layer being disposed immediately over said via holes in the lower layer.

43. The multilayer printed circuit board according to any of Claims 40 to 42 which comprises bumps formed immediately above said plated-through holes.

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44. The multilayer printed circuit board according to any of Claims 40 to 43 wherein said lower-layer via holes are filled with metal.

45. The multilayer printed circuit board according to

any of Claims 40 to 42 wherein valleys of said lower-layer via holes are filled with a conductive paste.

46. The multilayer printed circuit board according to any of Claims 40 to 42 wherein valleys of said lower-layer via holes are filled with a resin.

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